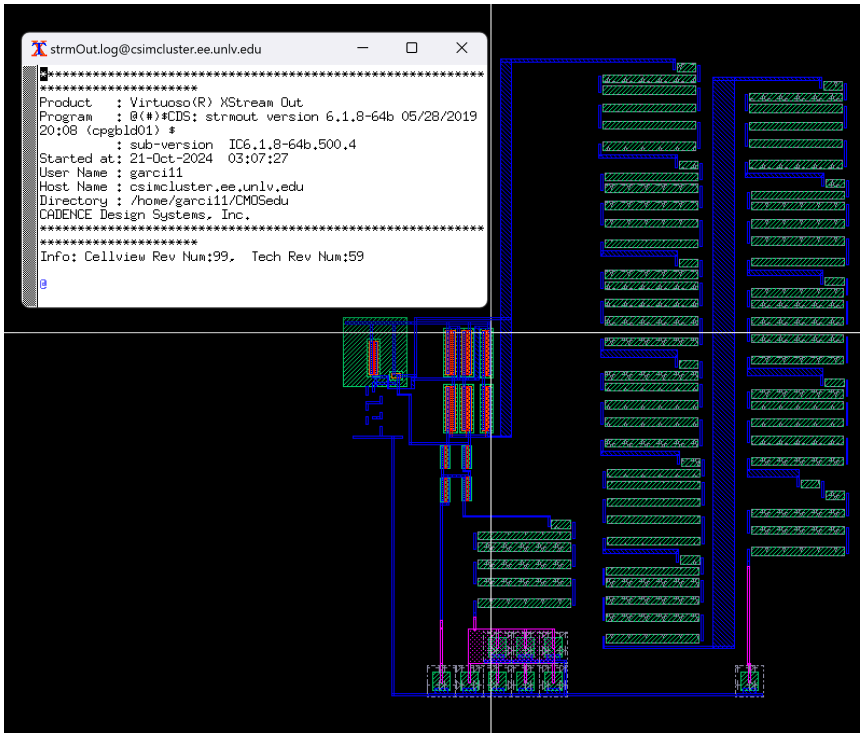
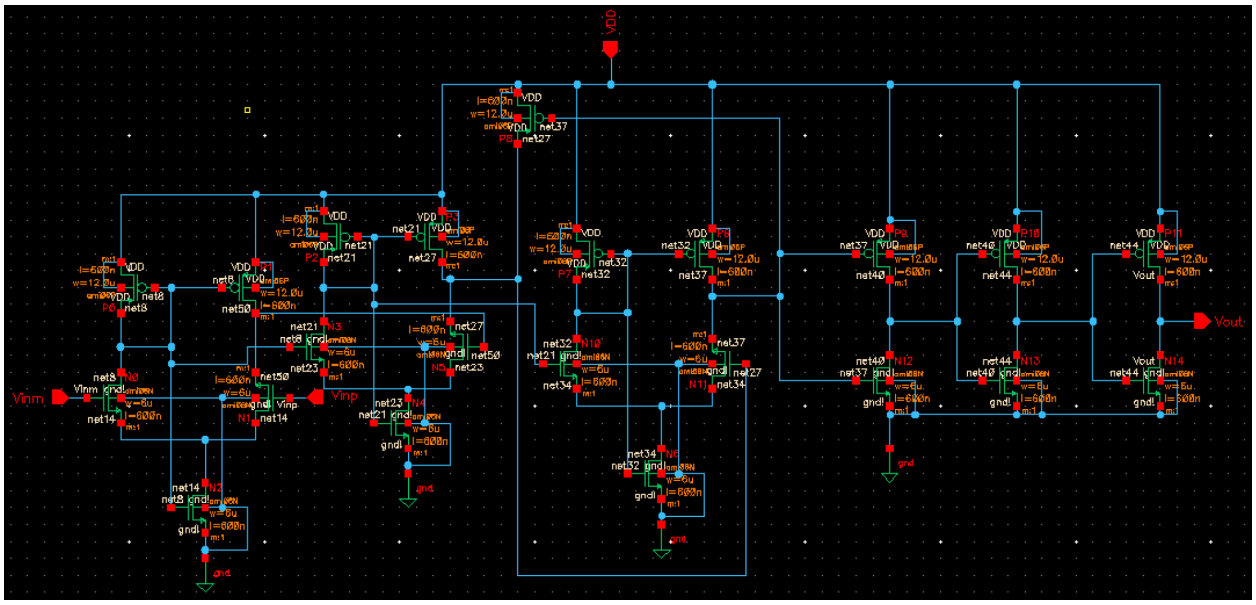
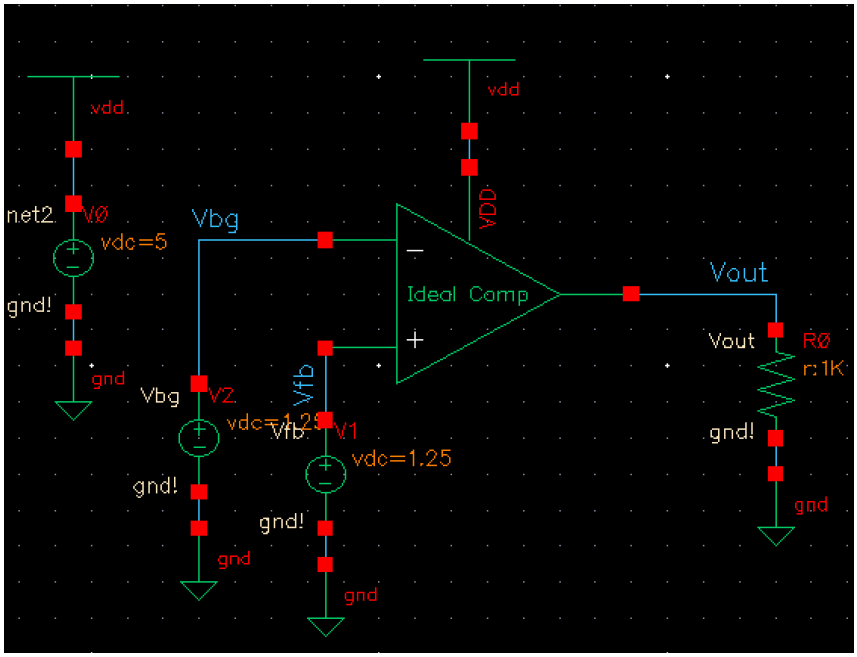
Abraham Garcia
EE 421 Project



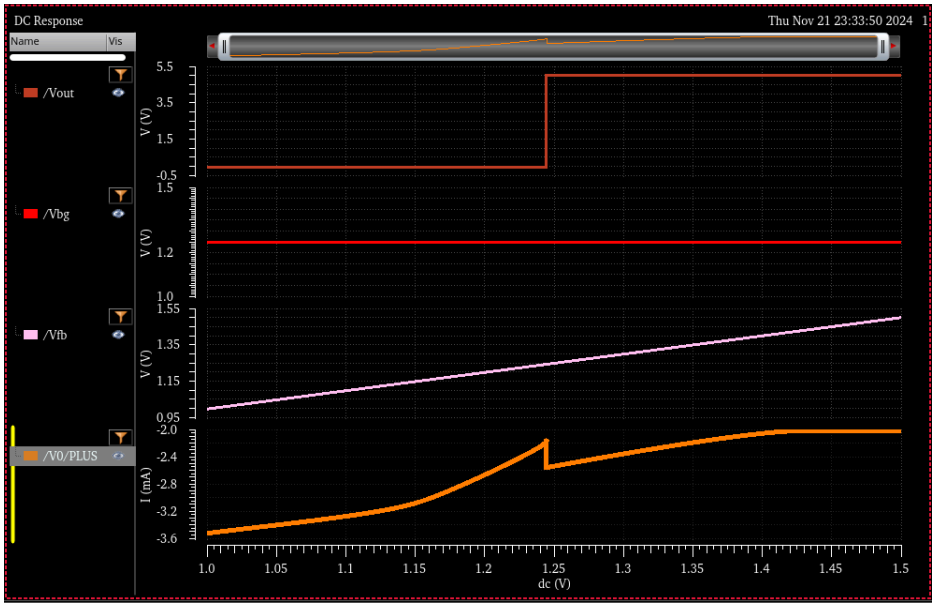
The bandgap reference circuit stabilizes the voltage reference against changes in temperature by combining two opposing temperature dependent voltages.

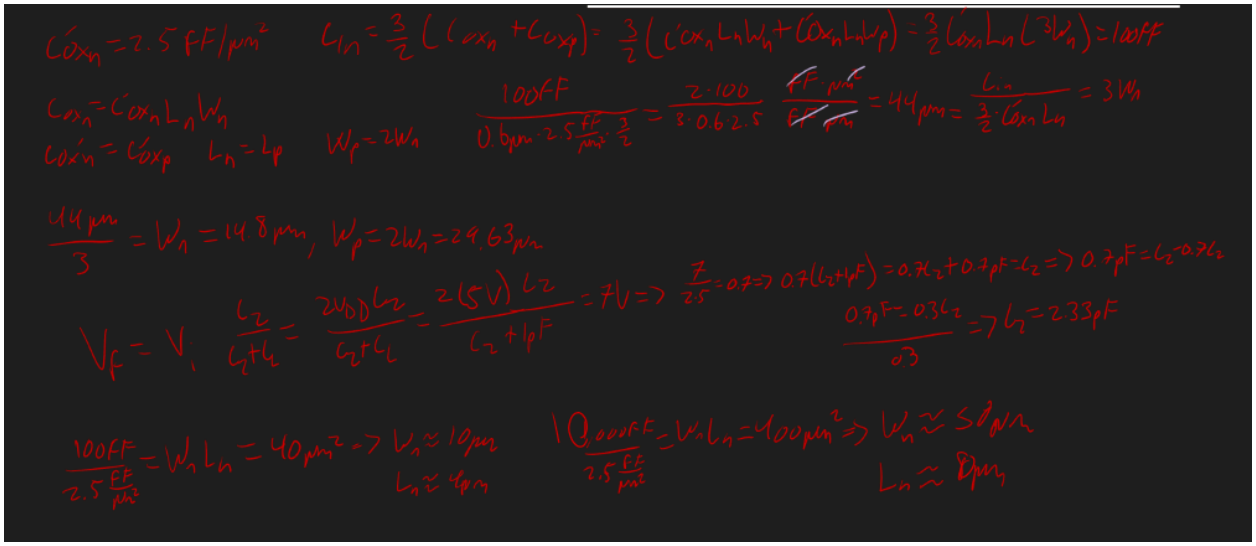


The circuit compares two input voltages, Vin- and Vin+, to determine Vout. For the buck converter it is used to compare the voltage feedback with the voltage reference from the bandgap. if Vfb < Vref Vout goes low , 0V, if Vfb > Vref then Vout goes high, 5V.

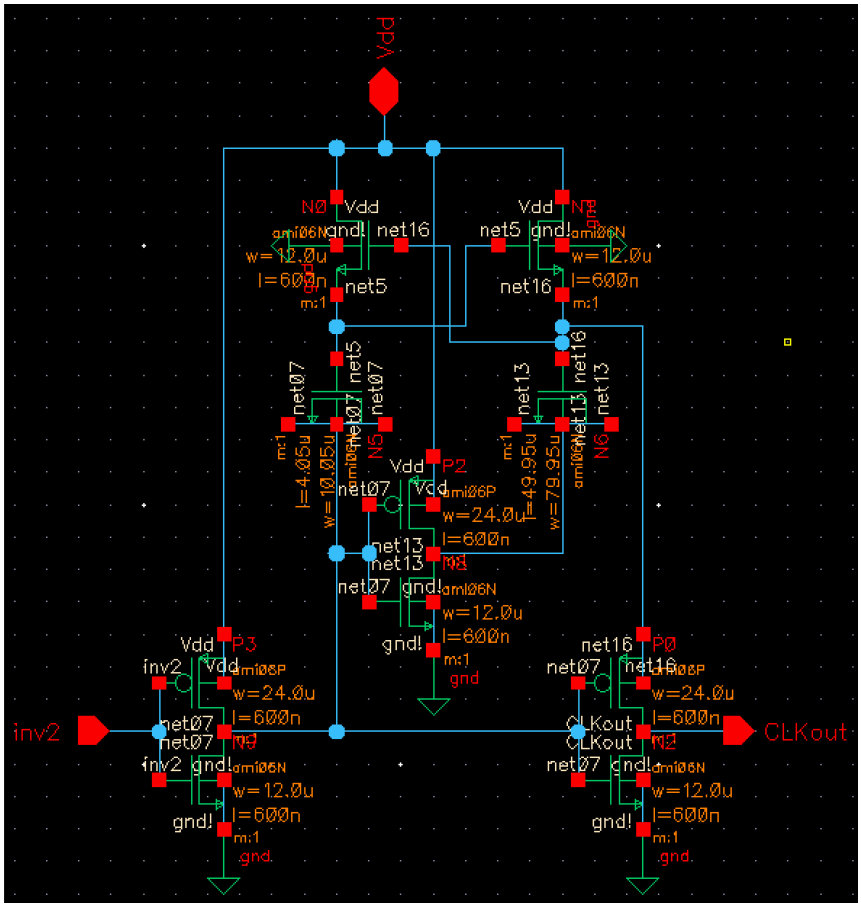


Here we simulate the comparator with a Vfb reference voltage to an ideal feedback of 1.25V to display the Vout sharp rise from 0V to 5V as Vfb rises from Vfb<Vbg to Vfb>Vbg.



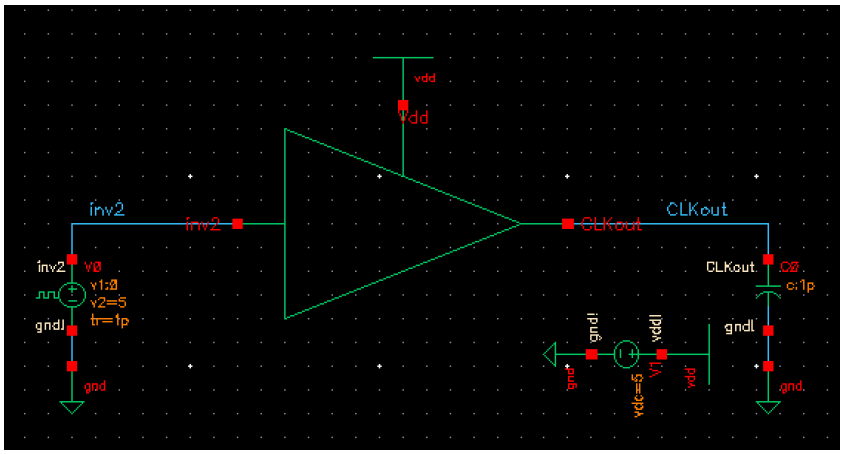


Here we calculated the NMOS capacitor for the left and right capacitor of the charge pump. Using the C5 process we used to get Wn about 10um and Ln about 4um for the 100fF on the left, and Wn about 50um and Ln about 80um for the right capacitor of 10pF.

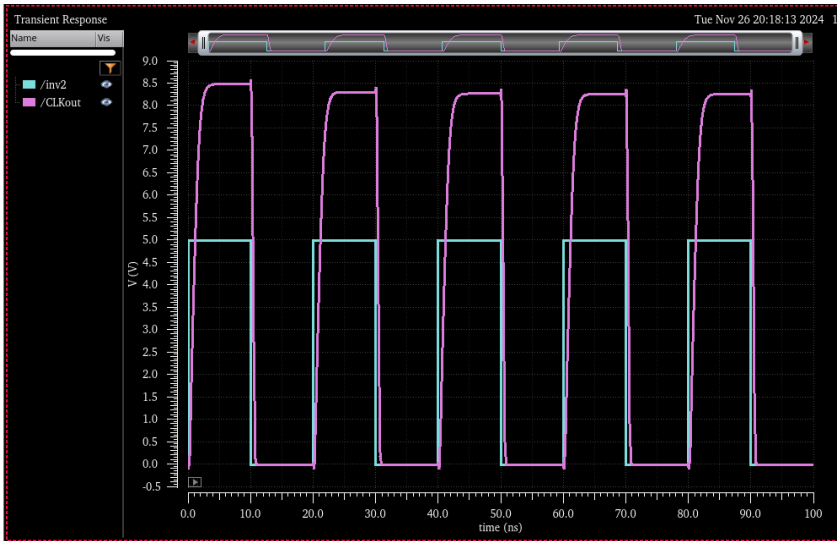


The charge pump outputs nearly double the input voltage by using an inverter at both the beginning and end. For example, with a pulse input voltage alternating between 0V low and 5V high: when the input is 0V, it is inverted to 5V, charging the left capacitor. This charge is then

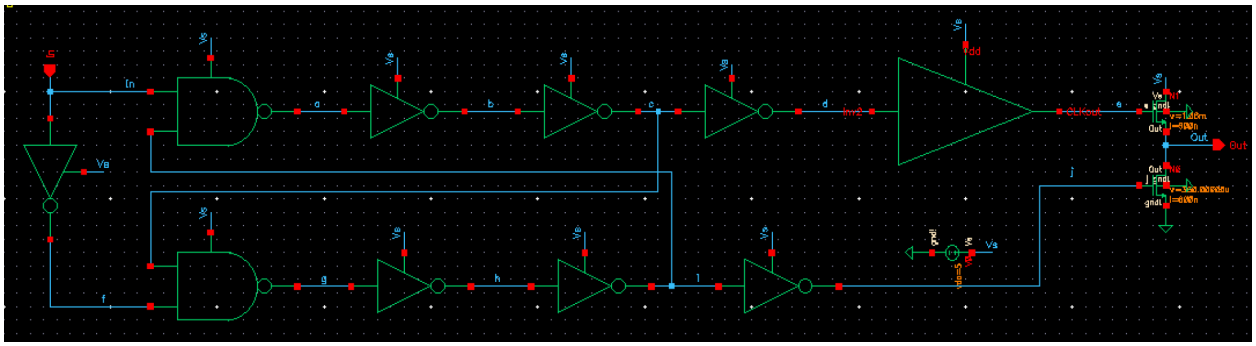
used to drive the gate of the right NMOS, allowing 5V to flow and charge the right capacitor. In the next clock cycle, when the input voltage is 5V and inverted to 0V, the inverter between the two capacitors flips it back to 5V. This process doubles the voltage on the right capacitor to approximately 2VDD, which is fed to the inverter's Vs. With the gate at 5V, this allows Vs = 2VDD to appear at the output.



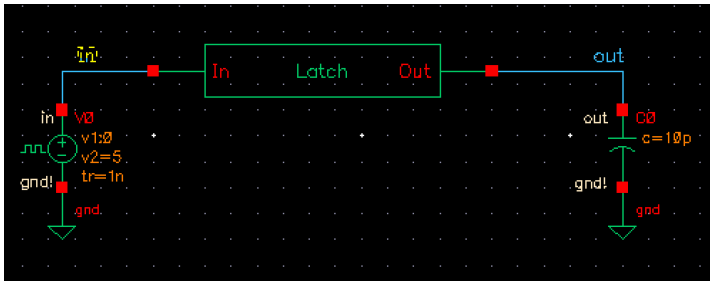
Here I simulated the charge pump with a 1pF capacitor at the end with an input Vpulse of 0V to 5V, 1ps rise and fall, and 10ps width and 20ps period.



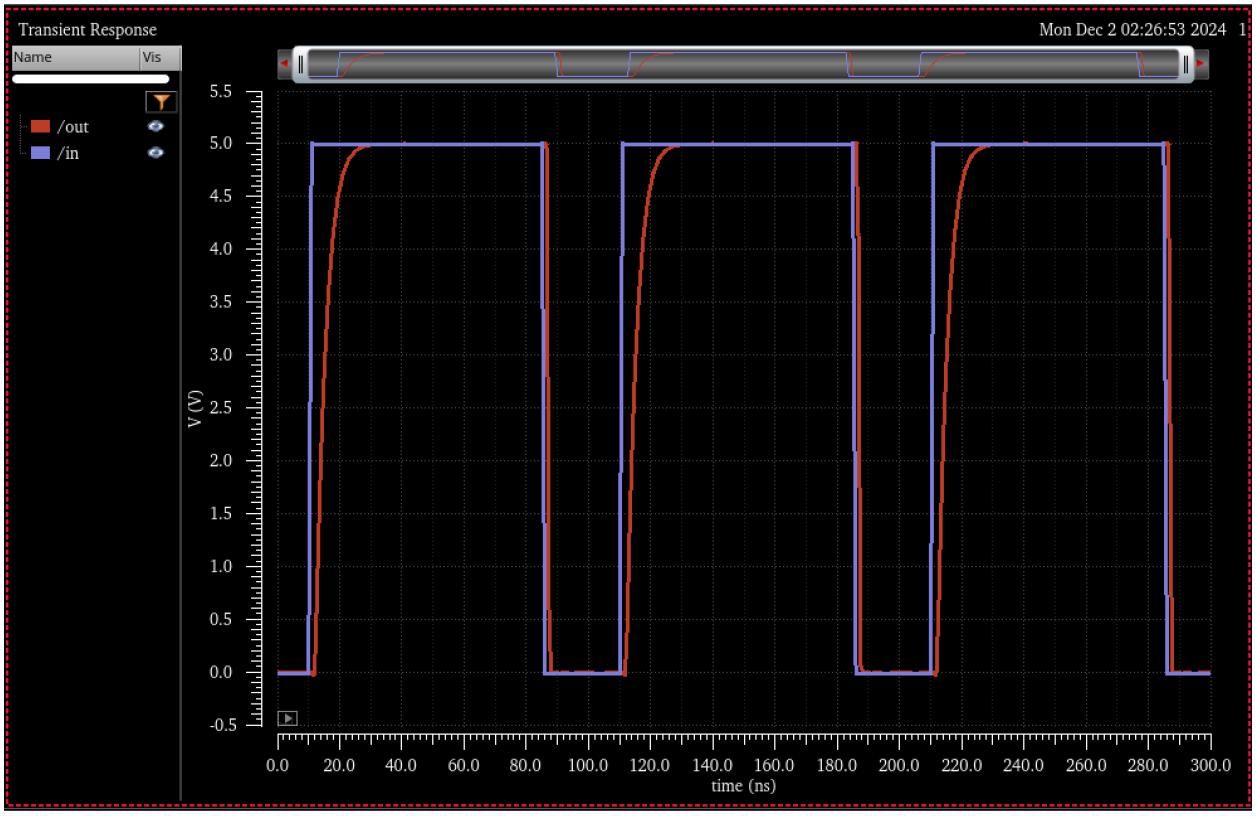
Here shows my output with Vin/inv2 being 5V-0V and Vout/CLKout 8.5V-0V.



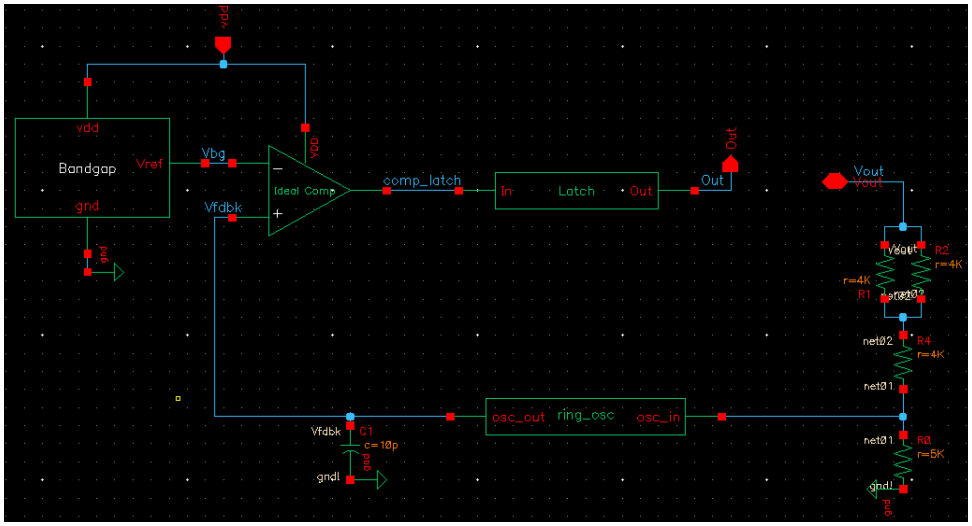
I then added the charge pump to the latch with inverters and nand2 using 12u/6u for pmos/nmos width. I added two NMOS at the end, the NMOS below being 360u/0.6u and 15u/0.6u for the top NMOS.



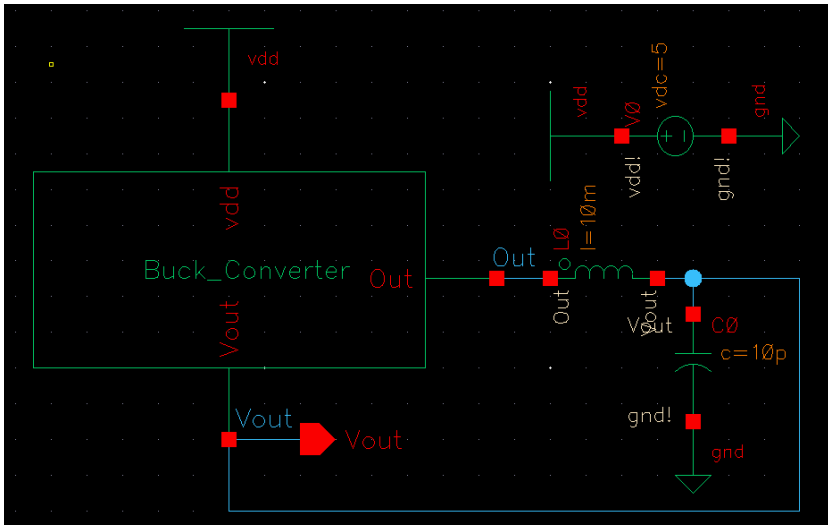
The latch stores and keeps logic states using inverters and nand2 gates with feedback paths. It uses a pulsing input signal to determine whether to propagate current input to output or to hold previous state. The nand gates control the signal flow while the inverters add delay and synchronize the outputs. The feedback loop holds onto the previous state when the input pulse is low. The two NMOS stabilizes the output.

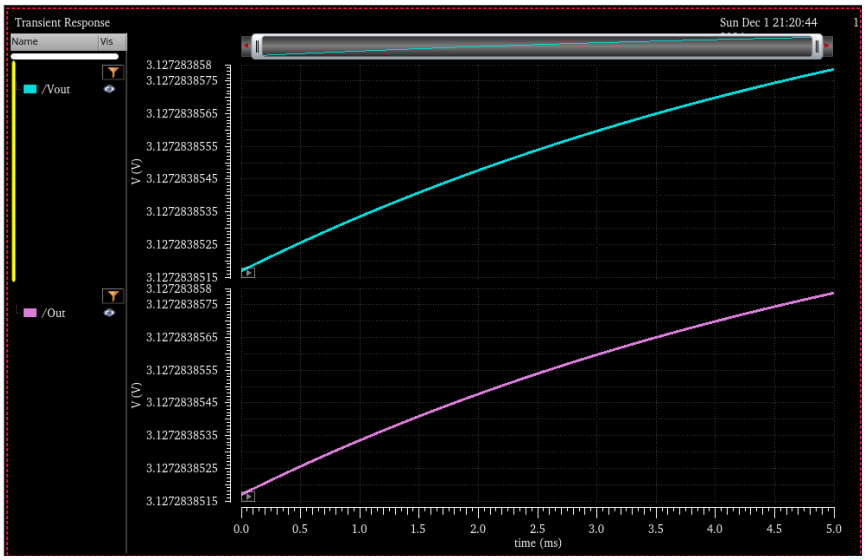


After that I created the oscillator by connecting 37 inverters together to filter the noise in the feedback voltage signal.

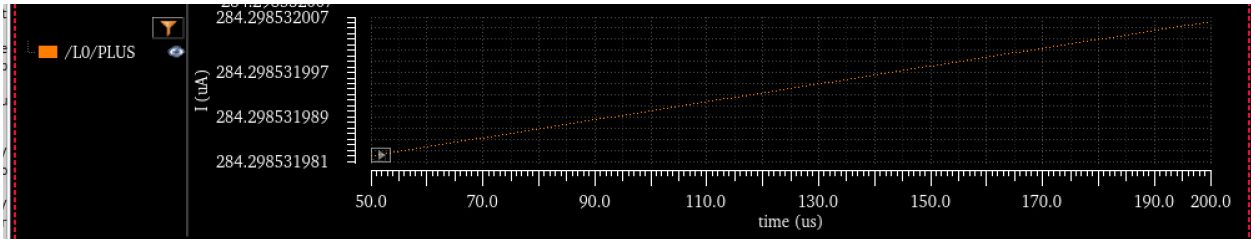


I then created the buck converter as shown above to compare the feedback voltage to the bandgap voltage reference to determine whether to send a high, 5V, or low, 0V, signal into the latch to ensure there is no overlap between MU and MD signals which feeds into output pin Out. Which connects to the inductor then to a parallel capacitor which leads to ground and resistor which leads into the oscillator which is parallel to a resistor to ground. The resistor, inductor and capacitor filters the signal further for a clean signal.

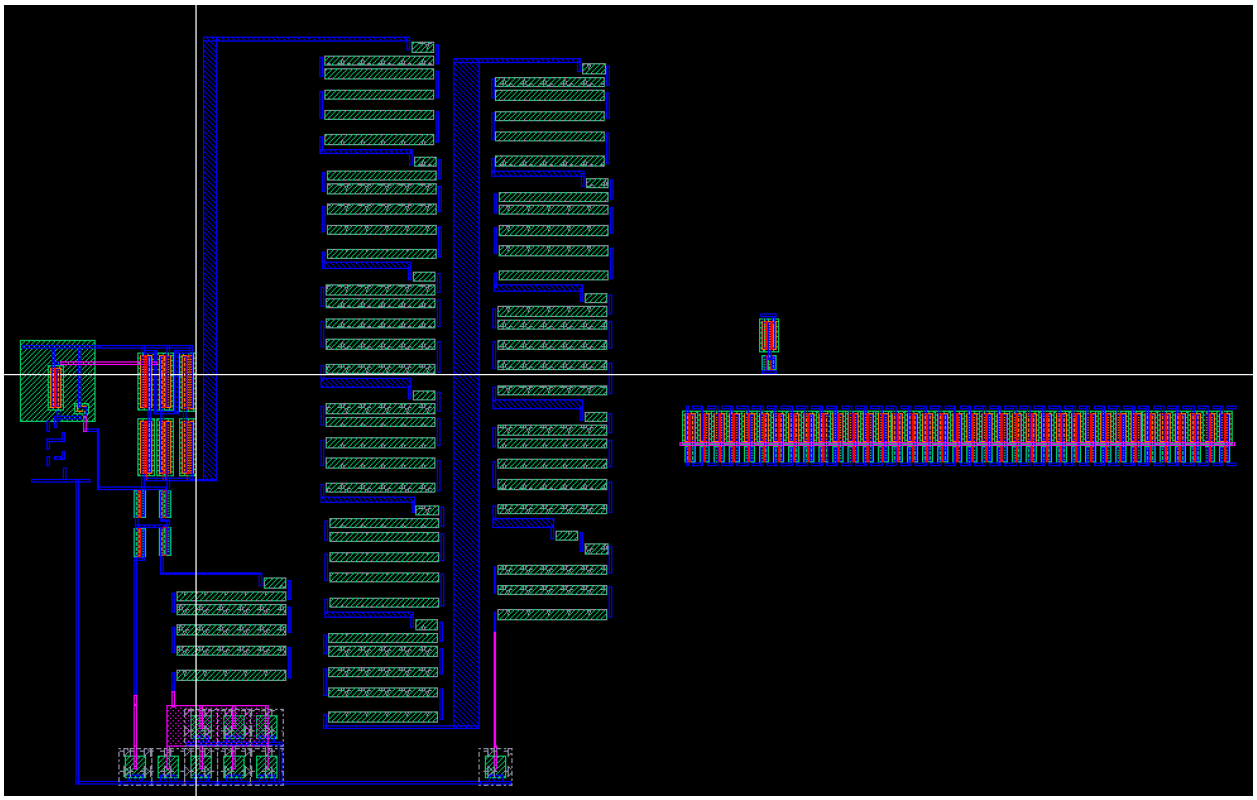




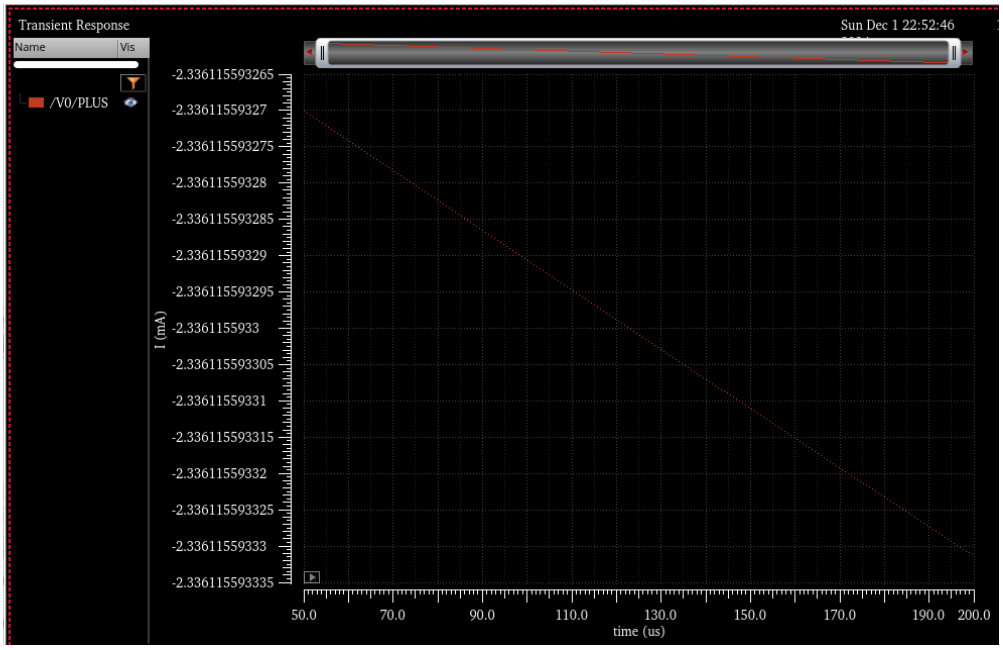
Vout and Out voltage around 3.127V



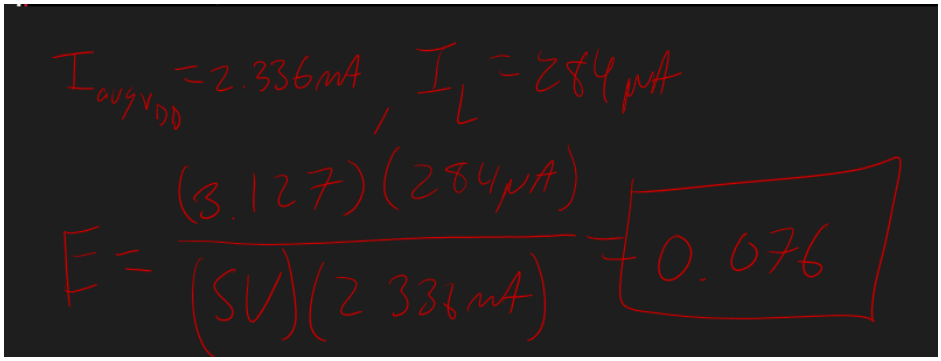
Current from the inductor.



The buck converter layout with the bandgap on the right and the oscillator on the bottom left and the nand2 layout on the top right.



Iavg$_{VDD}$ current.



Here is the efficiency score of 0.076 I wasn't able to manage to bring the current down to the requirement of 10uA-50uA.